Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A network interface, comprising:

a direct memory access unit;

a network data transmit path to couple a host system to a network, the network data transmit path leading to the network; and

circuitry to:

receive and transmit network data for a host processor of the host system, the transmitting network data via the network data transmit path to the network;

intercept from among network data in the network data transmit path one or more packets from said host processor;

generate, based on the receiving and transmitting network data, a set of statistics metering operation of the network interface, the set of statistics including at least one selected from the group of: (1) a number of bytes received, and (2) a number of packets received;

periodically initiate direct memory access transfers of the set of statistics from the network interface to a memory of the host system accessible by the host processor, wherein the circuitry to initiate the direct memory access transfers at a periodicity of a time interval value; and

configure said initiation of the direct memory access transfers using a configuration information, wherein the circuitry to determine said configuration information from a payload of said one or more packets, wherein said configuration information comprises said time interval value.

2. (Previously Presented) The network interface of claim 1, wherein the set of statistics comprises each of the following: a number of packets received by the interface, a number of bytes received by the interface, a number of packets transmitted by the interface, and a number of bytes transmitted by the interface.

3. (Previously Presented) The network interface of claim 2, wherein the circuitry comprises circuitry to include a timestamp with the direct memory access transfer of the set of statistics, the timestamp being a time when values of the set of statistics transferred by direct memory access were set by the network interface.

4. (Previously Presented) The network interface of claim 2, wherein the circuitry comprises circuitry to include a sequence count with the direct memory access transfers of the at least one statistic, the sequence count sequentially numbering successively DMA-ed sets of the statistic.

5. (Previously Presented) The network interface of claim 1, wherein the set of statistics comprises multiple RMON (Remote Monitoring) statistics.

6. (Previously Presented) The network interface of claim 1, wherein the circuitry comprises circuitry to initiate direct memory access transfer of received network data.

7. (Original) The network interface of claim 1, wherein the network interface comprises a framer.

8. (Original) The network interface of claim 7, wherein the network interface comprises a Media Access Controller (MAC).

9. (Original) The network interface of claim 1, wherein the network interface comprises a PHY.

Claims 10 and 11. (Canceled).

12. (Original) The network interface of claim 10, wherein the circuitry to configure comprises at least one register.

13. (Previously Presented) The network interface of claim 1, wherein the circuitry to configure comprises circuitry to determine from said configuration information a first location in the memory for a first direct memory access transfer and a second location in the memory, different from the first location, for a second direct memory access transfer.

14. (Previously Presented) The network interface of claim 13, wherein the circuitry to periodically initiate direct memory access transfers comprises circuitry to:

initiate the first direct memory access transfer based on the determining the first location, the first direct memory access transfer to transfer to the first location data indicating a first value of a statistic at a first time; and

initiate, after the first direct memory access transfer, the second direct memory access transfer based on the determining the second location, the second direct memory access transfer to transfer to the second location data indicating a second value of the statistic at a second time.

15. (Original) The network interface of claim 1, wherein the direct memory access unit comprises circuitry to notify a processor of completion of a transfer.

Claims 16 -38. (Canceled).

39. (Previously Presented) The network interface of claim 14, wherein the memory of the host system comprises a ring including the first location and the second location, the ring to store snapshots of counter values of the network interface.

40. (Previously Presented) The network interface of claim 14, wherein the first location is appended to a linked list after the first direct memory access transfer, and wherein the second location is appended to the linked list after the second direct memory access transfer.

41. (Previously Presented) The network interface of claim 1, wherein the circuitry to determine said configuration information from the payload of said one or more packets includes circuitry to identify information in the one or more packets indicating that the one or more packets are not to be transmitted over the network.